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LISTING OF CLAIMS

1. (Previously Presented) A graphics processing module, comprising:
a graphics processing unit;
a clock generator configured to generate a clock signal; and
a controller coupled to the clock generator, wherein the controller is configured to receive the clock signal, compare the clock signal with a synchronization signal to generate a timing signal, and transmit the timing signal to a second graphics processing module.
2. (Previously Presented) The graphics processing module of claim 1, wherein the graphics processing module is configured to generate a first portion of an image and the second graphics processing module is configured to generate a second portion of the image such that the first portion and the second portion synchronously form the image.
3. (Previously Presented) The graphics processing module of claim 1, wherein the controller is further configured to transmit the timing signal to the graphics processing unit.
4. (Previously Presented) The graphics processing module of claim 1, wherein the controller is configured to transmit the timing signal to the graphics processing unit and the second graphics module in response to the clock signal and the synchronization signal being in phase.
5. (Previously Presented) The graphics processing module of claim 1, wherein the synchronization signal is an external synchronization signal.
6. (Previously Presented) The graphics processing module of claim 1, wherein the controller is further configured to transmit a stereo field signal to the second graphics processing module.

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7. (Previously Presented) The graphics processing module of claim 1, wherein the graphics processing unit further comprises:
- a frame buffer having a front portion and a back portion; and
 - a swap ready input/output element through which a swap ready signal is communicated to the second graphics processing module, wherein the swap ready signal indicates to the second graphics processing module that an image content stored in the back portion of the frame buffer is ready to be transferred to the front portion of the frame buffer.
8. (Previously Presented) The graphics processing module of claim 7, wherein the frame buffer is configured to generate the swap ready signal in response to a completed transfer of the image content from the back portion to the front portion.
9. (Previously Presented) The graphics processing module of claim 7, wherein the frame buffer is configured to generate the swap ready signal in response to a soon to be completed transfer of the image content from the back portion to the front portion.
10. (Previously Presented) The graphics processing module of claim 1, wherein the controller is further configured to supply a vertical timing reset signal to the graphics processing unit.
11. (Previously Presented) The graphics processing module of claim 1, wherein the controller is further configured to supply a horizontal timing reset signal to the graphics processing unit.
12. (Previously Presented) The graphics processing module of claim 1, wherein the graphics processing unit further comprises a vertical timing reset signal counter configured to keep track of the number of vertical timing reset signals for use in deriving a frame count.
13. (Previously Presented) The graphics processing module of claim 12, wherein the controller is further configured to provide the frame count to the second graphics processing module.

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14. (Previously Presented) A graphics processing module, comprising:
a graphics processing unit;
means for generating a clock signal; and
means for receiving the clock signal, comparing the clock signal with a
synchronization signal to generate a timing signal; and transmitting the timing signal to a
second graphics processing module.
15. (Previously Presented) The graphics processing module of claim 14, wherein
the graphics processing module is configured to generate a first portion of an image and
the second graphics processing module is configured to generate a second portion of
the image such that the first portion and the second portion synchronously form the
image.
16. (Previously Presented) The graphics processing module of claim 14, wherein
the synchronization signal is an external synchronization signal.
17. (Previously Presented) The graphics processing module of claim 14, further
comprising means for transmitting a stereo field signal to the second graphics
processing module.
18. (Previously Presented) The graphics processing module of claim 14, wherein
the graphics processing unit further comprises:
means for buffering an image content; and
means for providing a swap ready signal to the second graphics processing
module to indicate to the second graphics processing module that the image content is
ready to be transferred from a back portion to a front portion of the buffering means.
19. (Previously Presented) The graphics processing module of claim 14, wherein
the graphics processing unit further comprises means for keeping track of the number of
vertical timing reset signals for use in deriving a frame count.

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20. (Previously Presented) The graphics processing module of claim 19, further comprising means for sending the frame count to the second graphics processing module.
21. (Previously Presented) A graphics system, comprising:
a first graphics processing module having:
a graphics processing unit,
a clock generator configured to generate a clock signal, and
a controller coupled to the clock generator, wherein the controller is configured to receive the clock signal, compare the clock signal with a synchronization signal to generate a timing signal, and transmit the timing signal;
and
a second graphics processing module coupled to the first graphics processing module, wherein the second graphics processing module is configured to receive the timing signal from the first graphics processing module.
22. (Previously Presented) The graphics system of claim 21, wherein the first graphics processing module is configured to display a first portion of an image and the second graphics module is configured to display a second portion of the image, wherein the first portion and the second portion synchronously form the image.
23. (Previously Presented) The graphics system of claim 21, wherein the controller is further configured to transmit a stereo field signal from the first graphics processing module to the second graphics processing module.
24. (Previously Presented) The graphics system of claim 21, wherein the graphics processing unit further comprises:
a frame buffer having a front portion and a back portion; and
a first swap ready input/output element configured to transmit a swap ready signal to the second graphics processing module, wherein the swap ready signal indicates whether an image content stored in the back portion of the frame buffer is ready to be transferred to the front portion of the frame buffer.

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25. (Previously Presented) The graphics system of claim 21, wherein the graphics system is implemented on a silicon substrate.